専攻セミナーのご紹介（7 月 13 日（月曜日）　16：30－17：30　Cisco Webex Meetings）

筑波大学の CiC パートナーであるグルノーブル大学は，筑波大学に研究室を設置，筑波大との交流を行っています [1]．今回，グルノーブル大学，LTM-CNRS，CEA-LETI[2]に所属する Marceline Bonvalot 先生に Cisco Webex Meetings を利用して，講演して頂くことになりました．Bonvalot 先生はグルノーブル CiC に所属，筑波大で講義，共同研究されている C. Vallée 先生（数理物質系）の共同研究者で，主に原子層堆積（Atomic Layer Depositon：ALD）の開発に従事されています．ご講演でも，ALD の最近の動向，最新の ALD および ALE(Atomic Layer Etching)を組みあわせた超微細構造デバイスのプロセスについてお話し頂く予定です．お忙しい中，たいへん恐縮ですが，ご参加頂ければ幸いです．また，今後のグルノーブル CiC グループ（副 PI：C. Mannequin 先生）と筑波大学の共同研究テーマ等についてもご検討ください．

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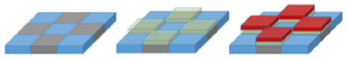
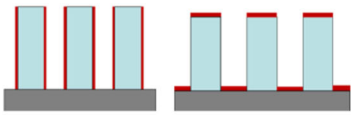
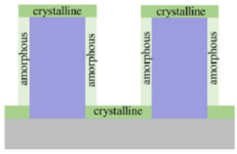
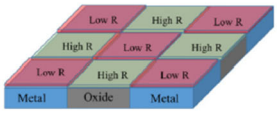
参考：

[1] http://www.global.tsukuba.ac.jp/partner/grenoble-cic?language=ja

[2] https://hal.archives-ouvertes.fr/LTM

（本セミナーは TREMS との共催です）

Form Vallée *et al.*, J. Vac. Sci. Technol. A38, 033007 (2020)

| Selective process | Definition | Example |
|---|---|---|
| Area selective deposition (chemically selective deposition) | Deposition on chemically selected surfaces and not others |  |
| Topographically selective deposition | Deposition in a pre-determined space direction only |  |
| Chemical/structural selective deposition | Different compositions or structures on one desired surface or space direction |  |
| Properties selective deposition | Different material properties on one desired surface or space direction |  |

**Advances in nanoelectronics fabrication technologies : Area Selective Deposition processes for innovative nano-patterning applications**

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FRANCE

For more than 50 years, the microelectronics industry has been driven at a constant miniaturization pace for the fabrication of smaller devices with increased functionalities, essentially relying on photolithography processing steps. However, with device dimensions nowadays reaching the nanoscale size, several photolithography patterning steps are required, such as Self Aligned Double or Quadruple Patterning (ASDP, SAQP), with atomic-scale alignment control to minimize associated placement errors. This generates numerous wafer handling steps and exponentially raises associated fabrication costs. Therefore, a general consensus emerges, which stipulates that a new fabrication paradigm based on bottom-up solutions be searched for and developed in order to sustain continuous downscaling of microelectronics devices [1].

In this regard, our group has developed an original nanoscale patterning facility, which combines Plasma Enhanced Atomic Layer Deposition (PEALD) and Atomic Layer Etching (ALE) possibilities in only one experimental tool. It consists in a standard PEALD reactor equipped with an Inductively Coupled Plasma (ICP) source and an additional substrate biasing system to enable the definition of super-cycles alternating not only atomic scale deposition and etching steps, but also *in situ* surface passivation and activation treatments and inert or reactive ion sputtering steps. This unique reactor configuration opens up the way to numerous experimental strategies and significantly expands the toolbox available for the definition of Area and Topographical Selective Deposition (ASD, TSD) processes [2].

In this talk, after a short description of the tool that we have conceived for this purpose, I will discuss a few strategic routes for the bottom-up definition of nanoscale patterns, both on 2D and 3D substrates. Proofs of concept will be shown for the selective deposition of TiN on vertical and horizontal sidewalls only, in 3D structures with aspect ratio less than 10. The conformality issue of Plasma Enhanced ALD processes in high aspect-ratio 3D structures will be addressed by discussing the impact of energetic ions extracted from the plasma, thanks to a careful adjustment of the substrate bias.

[1] : A. J. M. Mackus, M. J. M. Merkx and W. M. M. Kessels. *Chem. Mater* 31, 2-12, **2019**.

[2]: C. Vallée, M. Bonvalot, S. Belahcen, T. Yeghoyan, M. Jaffal, R. Vallat, A. Chaker, S. Lefèvre, S. David, A. Bsiesy, N. Possémé, R. Gassilloud, A. Granier. J. Vac. Soc. A38, 033007 **2020**.